IN THE CLAIMS

Please amend the claims as follows.

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1. (Amended) A method for detecting and decoding data comprising:

receiving a set of data signals from an external data source;

detecting a size of said received set of data signals;

decoding said received set of data signals;

extracting a destination address from said set of data signals;

comparing said destination address extracted from said data signals to a known data value;

determining whether said received data signals should be received by a host circuitry based upon said comparison of said destination address extracted from said data signals to a known data value;

generating at least one status signal alerting said host circuitry of said determination that said received data signals should be received by said host circuitry; and

waking up said host circuitry from a sleep mode upon a determination that said received set of data is addressed to said host circuitry.

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3. (Amended) The method as described in claim 2, wherein said step of detecting a size of said received set of data signal and decoding said received set of data signals, comprises:

converting said serial data packet into a parallel data format;

extracting a word clock from said received data packet;

incrementing a number held by said counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;

a2 using said word count to address data stored in a memory circuitry; and

inputting a set of data signals from said memory circuitry into an appropriate comparator.

10. (Amended) An apparatus for detecting and decoding data, comprising:

a data formatter;

a clock divider;

a3 a counter;

a host circuitry interface capable of transmitting and receiving data from a host circuitry, said host circuitry enter a wake up state from a sleep mode based upon data received by said host circuitry;

a memory circuitry;

a plurality of comparators;

a mask circuitry;

a digital logic circuitry;

a plurality of status registers; and

a plurality of clocked registers.

23. (Amended) A computer readable program storage device encoded with instructions that, when executed by a computer, performs a method, comprising:

receiving a set of data signals from an external data source;

a4 detecting a size of said received set of data signals;

decoding said received set of data signals;

extracting a destination address from said set of data signals;

comparing said destination address extracted from said data signals to a known data value;

determining whether said received data signals should be received by a host circuitry based upon said comparison of said destination address extracted from said data signals to a known data value;

generating at least one status signal alerting said host circuitry of said determination that said received data signals should be received by said host circuitry; and

a4 waking up said host circuitry from a sleep mode upon a determination that said received set of data is addressed to said host circuitry.

24. (Amended) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 23, wherein said set of data signal received is a data packet that is in a serial data format, over a network line.

25. (Amended) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 24, wherein said step of detecting a size of said received set of data signal and decoding said received set of data signals, further comprises:

converting said serial data packet into a parallel data format;

extracting a word clock from said received data packet;

incrementing a number held by said counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;

using said word count to address data stored in a memory circuitry; and

inputting a set of data signals from said memory circuitry into an appropriate comparator.

26. (Amended) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 25, wherein said act of extracting a destination address from said set of data signals further comprises slicing said parallel data such that at least one destination address data word is generated.

27. (Amended) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 25, wherein said method of comparing said destination address to a known data value further comprises:

performing a comparison function upon said converted, parallel set of data signals, and said set of data from said memory circuitry;

generating a digital comparator status signal in response of said performance of comparator function; and

clocking in said digital comparator data signal into a register.

28. (Amended) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 27, wherein said method of determining whether said received data signals should be received by a

host circuitry further comprises latching all output of said plurality of comparators into a digital logic circuitry.

29. (Amended) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 28, wherein said output of said comparators are not latched when a mask circuitry indicates that a particular frame of data is not compared.

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30. (Amended) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 28, wherein said method of generating a status signal alerting said host circuitry further comprises performing an OR function upon all said latched output of said comparators.

31. (Amended) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 23, wherein said method of waking up said host circuitry further comprises generating a status signal alerting said host that a address match has been found.

32. (New) A method, comprising:

receiving a data signal;

extracting a destination address based upon said data signal to determine whether a host circuitry is being addressed by comparing said destination address to a predetermined address; and

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waking up a host circuitry from a sleep mode based upon said determination that said host circuitry is being addressed.

33. (New) The method of claim 32, wherein extracting said destination address further comprises:

converting a serial data packet from said received data into a parallel data format;

extracting a word clock from said received data packet;

as incrementing a number held by said counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;

using said word count to address data stored in a memory circuitry;

inputting a set of data signals from said memory circuitry into an appropriate comparator; and

extracting said destination address by slicing said parallel data such that at least one destination address data word is generated.

34. (New) An apparatus, comprising a controller to:

receive a data signal;

extract a destination address based upon said data signal to determine whether a host circuitry is being addressed by comparing said destination address to a predetermined address; and

wake up a host circuitry from a sleep mode based upon said determination that said host circuitry is being addressed.

35. (New) The apparatus of claim 34, further comprising:

a data formatter capable of converting a serial stream of data into parallel data words and detecting an end of a data stream;

a counter to receive parallel formatted data from said data formatter;

a clock divider capable of incrementing a count held by said counter;

a memory circuitry comprising a memory element and a memory data access logic;

a plurality of comparators to receive parallel formatted data from said data formatter;

a plurality of clocked registers;

a mask circuitry capable of preventing a registering of said comparator output into said clocked registers; and

a plurality of status registers to latch an output from said comparators.